

WHAT IS CLAIMED IS:

- 1 1. A pulse width modulation amplifier which
2 supplies to a load circuit an amplified output having
3 been subjected to a pulse width modulation,
4 comprising:
- 5 a first series circuit including a first
6 switching element connected to a positive pole side
7 of a first direct-current power source, and a second
8 switching element, one end of said load circuit being
9 connected to a connecting point between said first
10 switching element and said second switching element,
- 11 a second series circuit including a third
12 switching element connected to a positive pole side
13 of a second direct-current power source, and a fourth
14 switching element, the other end of said load circuit
15 being connected to a connecting point between said
16 third switching element and said fourth switching
17 element, and
- 18 a driving circuit which turns on a set of said
19 first switching element and said fourth switching
20 element, and a set of said second switching element
21 and said third switching element, set-by-set, each of
22 said sets being alternately put into on-state.

1 2. A pulse width modulation amplifier which supplies
2 to a load circuit an amplified output having been
3 subjected to a pulse width modulation, comprising:

4 a first bridge circuit having a series circuit
5 connecting the first switching element and the
6 second switching element, and a series circuit
7 connecting the third switching element being
8 connected to said first switching element, and the
9 fourth switching element, a connecting point
10 between said first and said third switching element
11 being connected to a first direct-current power
12 source, and a connecting point between said first
13 and said second switching elements being connected
14 to a connecting point between said third and said
15 fourth switching element by way of said load
16 circuit,

17 a second bridge circuit having a series circuit
18 connecting the fifth switching element and the sixth
19 switching element, and a series circuit connecting
20 the seventh switching element being connected to
21 said fifth switching element, and the eighth
22 switching element, a connecting point between said
23 fifth and said seventh switching elements being
24 connected to a second direct-current power source,
25 and a connecting point between said fifth and said
26 sixth switching elements being connected to a

27 connecting point between said seventh and said
28 eighth switching element by way of said load circuit,
29 and

30 a driving circuit which turns on a first set
31 of said first and fourth switching elements,

32 a second set of said second and third switching
33 elements, a third set of said fifth and eighth
34 switching elements and

35 a fourth set of said sixth and seventh switching
36 elements set-by-set, so that said first set and said
37 third set being alternately turned on, and between
38 the periods when said first set and said third are
39 in on-state, an ON period of said second set and an
40 ON period of said fourth set alternately existing.